

Embedded Technology 2009

FPGA Track Seminar



Embedded Technology 2009
Show Managing Office
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Background & Purpose

- Background
 - FPGA has become to a key device to design a wide range of embedded systems.
 - Larger density FPGA devices integrate multiple processors into a single chip.
 - New design/verification methodologies are required
 - FPGA devices are now creating new applications.
 - Lower power, Lower cost, Higher speed, and Higher density
- Purpose
 - FPGA Track Seminar provides updated and valuable information for FPGA based embedded system designs to the show attendees.
 - FPGA Track Seminar provides speaking opportunities to ET Exhibitors supplying FPGA devices or design tools.
- History
 - Launched in 2004
 - Implemented as a part of the official conference programs presented by the show organizer, JASA .
 - keeps excellent track records, in terms of number of attendees.

FPGA Track Seminar at ET2008

- Total 12 presentations were provided
- Day-1 : Nov. 20th, 2008 ---6 presentations

	Exhibitor	Title	Speaker	Attendees
1	Altera	The Basic and Trends of the Latest FPGA	Altera	149
2	Altera	Advantages of FPGA based Embedded System Design	Altera	137
3	Actel	Easy Design for Ultra Low Power FPGA	Actel	125
4	Xilinx/TED	Serial Transceiver Connection with FPGA	Xilinx	116
5	Xilinx/TED	High-Speed Memory Interface Solution for FPGA	TED	122
6	Xilinx/TED	High-Speed Development of Embedded System by Linux and FPGA	Atmark Techno	99

FPGA Track Seminars at ET2008

- Day-2 : Nov. 21st, 2008 ---another 6 presentations

	Exhibitor	Title	Speaker	Attendees
7	Xilinx/TED	FPGA Roadmap with New Processor Technology, and Product Trend	Xilinx	83
8	Xilinx/TED	Selection & Configuration Method of Power Supply for FPGA	TED	111
9	Actel	Analog Signal Control using Mixed Signal FPGA with Embedded Processor	Actel	92
10	Altera	AMP-based Multi-core System Design Example using FPGA	Euphonic	86
11	Altera	Using FPGAs for Embedded System Design	Olympus & Altera	126
12	Altera	Minimizing Noise & Jitters of High Speed Transceiver in 40nm FPGA	Altera	68

FPGA Track Seminar at ET2009

- Date: Nov. 19 and 20, 2009 (Tentative)
- Venue: Pacifico Yokohama, Annex Hall
- Sign-up & Fee: Free of charge seminar for both presenter & attendees.
- Registration: Pre-registration is required to attend each seminar.
- Length : 45 minutes presentation/unit
- Room capacity: 100 attendees accommodated in school style
- Time-slots: 12 slots in total
- Eligibility: Only the exhibitors at ET 2009 are eligible for the presenter at FPGA Track Seminar.
 - Number of time slots allocated to the presenters will be determined depending on the booth size.
 - FPGA device vendor/Distributor or Tool vendor
 - Programs will be decided by the organizer & ET2009 Executive Committee.

FPGA Track Seminar at ET2009

- Language: Japanese
 - Presentation should be provided in Japanese.
 - Please note that we do not offer simultaneous interpretation service.
- Handouts:
 - The presenter is required to prepare handout copies.
 - You may want to include datasheet & brochure along with handouts.
- Attendee's Contact info:
 - Due to the organizer's privacy policy, the contact list of attendees is not disclosed to the presenter side.
- Feedback of the seminar:
 - The organizer will give the presenter feedback obtained from the attendees.
 - Distribution of another questionnaire by presenter is not allowed.

Time Line

- Application for ET2009 begins : **April 1st, 2009**
- Application deadline: **June 30th, 2009**
 - Upon application, those wishing to sign up for FPGA Track Seminar are required to notice the organizer.
- Tentative seminar title & presenter info: By **July 31st, 2009**
 - Participants for FPGA Track Seminar are required to submit the seminar title and presenter info to the organizer by the above deadline date.
- Formal seminar title & presenter info: By **August 31th, 2009**
 - Participants for FPGA Track Seminar are required to submit the final draft (seminar title & presenter info) to the organizer.
- Seminar abstract deadline: **September 30th, 2009**

For Your Success

- Presentation title & abstract (400 characters in Japanese) can decide turnouts.
 - Try to give an impression of “pure technical seminar” by the title and abstract. This boosts engineers’ interest.
 - Avoid overly advertizing expressions which sound like product promotion because it will have an adverse effect on bringing engineers.
- Presentation by device or tool user is recommended.
- Distribution of a special ticket which is exchanged with attractive novelty goods will be effective to bring the seminar attendees to your booth.