

# Embedded Technology 2009

## Design & Verification Tool Track Seminar



Embedded Technology 2009  
Show Managing Office  
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# Background & Purpose

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- Today's complex embedded systems now require new design and verification methodologies and powerful tools for a software development
- Many new design and testing tools have been introduced

- Purpose

- “Design & Verification Tool Track” Seminar provides updated and valuable information for high level system design and verification process for embedded system designers
- “Design & Verification Tool Track” Seminar provides speaking opportunities to ET Exhibitors supplying these advanced tools

# “Design & Verification Track” Seminar at ET2009

- Date: Nov. 19 and 20, 2009 at (Tentative)
- Venue: Pacifico Yokohama, Annex Hall
- Sign-up & Fee: Free of charge seminar for both presenter & attendees.
- Registration: Pre-registration is required to attend each seminar.
- Length : 45 minutes presentation/unit
- Room capacity: 100 attendees accommodated in school style
- Time-slots: 12 slots in total
- Eligibility: Only the exhibitors at ET 2009 are eligible for the presenter at “Design & Verification Track” Seminar.
  - Number of time slots allocated to the presenters will be determined depending on the booth size.
  - Tool vendor, Distributor or User
  - Speakers and Program will be decided by the organizer & ET2009 Conference Committee.

# “Design & Verification Track” Seminar at ET2009

- Language: Japanese
  - Presentation should be provided in Japanese.
  - Please note that we do not offer simultaneous interpretation service.
- Handouts:
  - The presenter is required to prepare handout copies.
  - You may want to include datasheet & brochure along with handouts.
- Attendee's Contact info:
  - Due to the organizer's privacy policy, the contact list of attendees is not disclosed to the presenter side.
- Feedback of the seminar:
  - The organizer will give the presenter feedback obtained from the attendees.
  - Distribution of another questionnaire by presenter is not allowed.

# Time Line

- Application for ET2009 begins : **April 1<sup>st</sup>, 2009**
- Application deadline: **June 30<sup>th</sup>, 2009**
  - Upon application, those wishing to sign up for Design & Verification Track Seminar are required to notice the organizer.
- Tentative seminar title & presenter info: By **July 31<sup>st</sup>, 2009**
  - Participants for FPGA Track Seminar are required to submit the seminar title and presenter info to the organizer by the above deadline date.
- Formal seminar title & presenter info: By **August 31<sup>th</sup>, 2009**
  - Participants for this seminar are required to submit the final draft (seminar title & presenter info) to the organizer.
- Seminar abstract deadline: **September 30<sup>th</sup>, 2009**

# For Your Success

- Presentation title & abstract (400 characters in Japanese) can decide turnouts.
  - Try to give an impression of “pure technical seminar” by the title and abstract. This boosts engineers’ interest.
  - Avoid overly advertizing expressions which sound like product promotion because it will have an adverse effect on bringing engineers.
- Presentation by tool user is recommended.
- Distribution of a special ticket which is exchanged with attractive novelty goods will be effective to bring the seminar attendees to your booth.